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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/618,284	07/11/2003	Peter Brookes	15114H-067600US	4798

20350 7590 01/09/2008

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EXAMINER	
ALHIJA, SAIF A	

ART UNIT	PAPER NUMBER
2128	

MAIL DATE	DELIVERY MODE
01/09/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/618,284	BROOKES ET AL.	
	Examiner	Art Unit	
	Saif A. Alhija	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,5-16,18,19 and 24-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5-16,18,19 and 24-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 5-16, 18-19, and 24-33 have been presented for examination.

Claims 2-4, 17, and 20-23 have been cancelled.

Response to Arguments

2. Applicant's arguments filed 17 October 2007 have been fully considered but they are not persuasive.

i) Following Applicants amendments and arguments the 101 rejections of the claims are withdrawn.

ii) Applicant argues that Lin does not disclose the software model for the software simulation is embedded in the hardware environment and runs ahead of the hardware simulation" as well as "the software model is recited to control the hardware simulation." Applicant further argues that Lin does not disclose the reference clock parameter presented in the claims as well as the resulting synchronization and control by software.

As stated previously, Column 8, Lines 20-45 reproduced below shows the SEmulation system of Lin encompasses numerous modes **including software controlling hardware simulation**. This cited section also shows the **software simulation embedded in a hardware environment**. Further, Figure 49 also shows **scheduling, priorities, and swapping which reads on one part of the simulation running ahead of or behind another**.

The SEmulation system and method, in accordance with the present invention, provide four modes of operation: (1) Software Simulation, (2) Simulation via Hardware Acceleration, (3) In-Circuit Emulation (ICE), and (4) Post-Simulation Analysis. At a high level, the present invention is embodied in each of the above four modes or various combinations of these modes as follows: (1) Software Simulation alone; (2) Simulation via Hardware Acceleration alone; (3) In-Circuit Emulation (ICE) alone; (4) Post-Simulation Analysis alone; (5) Software Simulation and Simulation via Hardware Acceleration; (6) Software Simulation and ICE; (7) Simulation via Hardware Acceleration and ICE; (8) Software Simulation, Simulation via Hardware Acceleration, and ICE; (9) Software Simulation and Post-Simulation Analysis; (10) Simulation via Hardware Acceleration and Post-Simulation Analysis; (11) Software Simulation, Simulation via Hardware Acceleration, and Post-Simulation Analysis; (12) ICE and Post-Simulation Analysis; (13) Software Simulation, ICE, Post-Simulation Analysis; (14) Simulation via Hardware Acceleration, ICE, Post-Simulation Analysis; and (15) Software Simulation, Simulation via Hardware Acceleration, ICE, and Post-Simulation Analysis. Other combinations are possible and within the scope of the present invention.

Further, Column 56, Line 37-Column 57, Line 16 of Lin is reproduced below. This section shows that the **SEmulation system allows both asynchronous and synchronous data inputs** depending upon which is enabled. **Further, the software kernel controls hardware model evaluation.**

FIG. 17 shows a basic building block of the hardware model in accordance with one embodiment of the present invention. For the register component, the SEmulation system uses a D-type flip-flop with asynchronous load control as the basic block for building both edge trigger (i.e., flip-flops) and level sensitive (i.e., latches) register hardware models. This register model building block has the following ports: Q (the output state); A_E (asynchronous enable); A_D (asynchronous data); S_E (synchronous enable); S_D (synchronous data); and of course, System.clk (system clock).

This SEmulation register model is triggered by a positive edge of the system clock or a positive level of the asynchronous enable (A_E) input. When either of these two positive edge or positive level triggering events occurs, the register model looks for the asynchronous enable (A_E) input. If the asynchronous enable (A_E) input is enabled, the output Q takes on the value of the asynchronous data (A_D); otherwise, if the synchronous enable (S_E) input is enabled, the output Q takes on the value of the synchronous data (S_D). If, on the other hand, neither the asynchronous enable (A_E) nor the synchronous enable (S_E) input is enabled, the output Q is not evaluated despite the detection of a positive edge of the system clock. In this way, the inputs to these enable ports control the operation of this basic building block register model.

The system uses software clocks, which are special enable registers, to control the enable inputs of these register models. In a complex user circuit design, millions of elements are found in the circuit design and accordingly, the SEmulator system will implement millions of elements in

> the hardware model. Controlling all of these elements individually is costly because the overhead of sending millions of control signals to the hardware model will take a longer time than evaluating these elements in software. However, even this complex circuit design usually calls for only a few (from 1–10) clocks and clocks alone are sufficient to control the state changes of a system with register and combinational components only. The hardware model of the SEmulator system uses only register and combinational components. The SEmulator system also controls the evaluation of the hardware model through software clocks. In the SEmulator system, the hardware models for registers do not have the clock directly connected to other hardware components; rather, the software kernel controls the value of all clocks. By controlling a few clock signals, the kernel has the full control over the evaluation of the hardware models with negligible amount of coprocessor intervention overhead.

With respect to the reference clock parameter, Column 58, Lines 45-62 of the reference states:

> As stated earlier, the SEmulation system has the complete model of the user's circuit design in software and some portions of the user's circuit design in hardware. As specified in the kernel, the software can detect clock edges that affect hardware register values. To ensure that the hardware registers also evaluate their respective inputs, the software/hardware boundary includes a software clock. The software clock ensures that the registers in the hardware model evaluate in synchronization with the system clock and without any hold-time violations. The software clock essentially controls the enable input of the hardware register components, rather than controlling the clock input to the hardware register components. The double-buffered approach to implementing the software clocks ensures that the registers evaluate in synchronization with the system clock to avoid race conditions and eliminates the need for precise timing controls to avoid hold-time violations.

This section recites the reference clock parameter with respect to the **software clock which controls the hardware components**. It is unclear and Applicants have not fully explained how the reference does not teach the recited limitations. Specifically, Applicants argue on the top of page 10 of their remarks that the

reference clock parameter results in synchronization and "avoiding getting undesirably ahead of the hardware simulation" which appears to be equally recited in the Column 58 citation presented above.

iii) Since no additional arguments were made regarding the 103 rejections of claims 13 and 27 the rejections are maintained.

iv) Examiner has cited particular columns and line numbers in the references applied to the claims for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

v) The Examiner respectfully requests, in the event the Applicants choose to amend or add new claims, that such claims and their limitations be directly mapped to the specification, which provides support for the subject matter. This will assist in expediting compact prosecution.

vi) Further, the Examiner respectfully encourages Applicants to direct the specificity of their response with regards to this office action to the broadest reasonable interpretation of the claims as presented. This will avoid issues that would delay prosecution such as limitations not explicitly presented in the claims, intended use statements that carry no patentable weight, mere allegations of patentability, and novelty that is not clearly expressed.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 5-12, 14-16, 18-19, 24-26, and 28-33 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Lin et al. "Coverification System and Method", U.S. Patent No. 6,389,379, hereafter referred to as Lin.

Regarding Claim 1:

Lin discloses A method in a hardware environment for validating a design for a system which comprises a software element, and first and second hardware components, the software element being for execution on the second hardware component, and the first and second hardware components being operable to interact with one another, the method comprising the steps of:

simulating operation of the first hardware component in a first simulation in a hardware environment; **(Figures 46-49. 1, 2, 3, 5, and 19. Column 27, Lines 45- Column 28, Lines 57)**

simulating the software element and the second hardware component in a second simulation using a software model embedded within the hardware environment; **(Figures 1, 2, 3, 5, and 19. Column 27, Lines 45- Column 28, Lines 57)**

running the second simulation asynchronously with, and ahead of, the first simulation, the software model of the second simulation being synchronized with the first simulation using a reference clock parameter that limits a maximum number of processor clock periods of the second simulation per period of a reference clock of the hardware environment; **(See section 2.ii above)**

controlling the first simulation using the software model in the second simulation that is running ahead of the first simulation, a socket allowing for communication between the software model and the first simulation; and

analyzing the first and second simulations to validate and validating the design for the system, **(See section 2.ii above)**

wherein the first simulation and the second simulation are implemented in separate processing threads within the hardware environment providing more rapid simulation of software instructions in the software model than the simulation of instructions in the first simulation. **(Figures 1, 2, 3, 5, and 19. Column 27, Lines 45- Column 28, Lines 57. Column 30, Lines 47-61)**

Regarding Claim 5:

Lin discloses A method as claimed in claim 1, further comprising:

performing operations in the first simulation to set up an inter-process communications protocol connection therein; **(Column 87, Lines 50-64)**

connecting the second simulation to the interprocess communications protocol connection in the first simulation; **(Column 87, Lines 50-64)**

connecting a software debugger to the second simulation; **(Abstract. Column 1, Lines 33-49)**

and controlling the first simulation from the software debugger via the second simulation using the interprocess communications protocol. **(Abstract. Column 1, Lines 33-49)**

Regarding Claim 6:

Lin discloses A method as claimed in claim 1, further comprising:

performing operations in the first simulation to set up an inter-process communications protocol connection therein; **(Abstract. Column 1, Lines 33-49. Column 87, Lines 50-64)**

connecting a software debugger to the communications protocol connection; **(Abstract. Column 1, Lines 33-49. Column 87, Lines 50-64)**

and controlling the first simulation from the software debugger using the inter-process communications protocol. **(Abstract. Column 1, Lines 33-49. Column 87, Lines 50-64)**

Regarding Claim 7:

Lin discloses A method as claimed in claim 5 or 6, wherein the inter-process communications protocol is TCP/IP and the connection is a TCP/IP socket. **(Abstract. Column 1, Lines 33-49. Column 87, Lines 50-64)**

Regarding Claim 8:

Lin discloses A method as claimed claim 1, wherein the second hardware component includes a processor. **(Column 11, Line 59 – Column 12 Line 2)**

Regarding Claim 9:

Lin discloses A method as claimed in claim 8, wherein the processor is an embedded processor. **(Column 11, Line 59 – Column 12 Line 2)**

Regarding Claim 10:

Lin discloses A method as claimed in claim 1, wherein the hardware component includes processor peripheral devices. **(Column 11, Line 59 – Column 12 Line 2)**

Regarding Claim 11:

Lin discloses A method as claimed in claim 10, wherein the peripheral devices are embedded. **(Column 11, Line 59 – Column 12 Line 2)**

Regarding Claim 12:

Lin discloses A method as claimed in claim 1, wherein the first simulation is implemented using a hardware description language (HDL) simulation environment. **(Figure 26)**

Regarding Claim 14:

Lin discloses A method as claimed in claim 1, wherein the first hardware component is a programmable logic device. **(Column 63, Lines 4-10)**

Regarding Claim 15:

Lin discloses A method in a hardware environment for controlling a simulation of a system using a software debugger, the simulation useful for validating a design of the system wherein the system comprises a software element, and first and second hardware components, the software element being for execution on the second hardware component and the first and second hardware components being operable to interact with one another, the method comprising the steps of:

simulating the first hardware component in a first simulation in the hardware environment; **(Figures 1, 2, 3, 5, and 19. Column 27, Lines 45- Column 28, Lines 57)**

simulating the software element and the second hardware component in a second simulation using a software model embedded within the hardware environment, the first simulation and the second simulation being implemented in separate processing threads within the hardware environment; **(Figures 1, 2, 3, 5, and 19. Column 27, Lines 45- Column 28, Lines 57)**

performing operations to set up an inter-process communications protocol connection; **(Abstract. Column 1, Lines 33-49. Column 87, Lines 50-64)**

connecting the software debugger to the software model of the second simulation embedded in the hardware environment; **(Abstract. Column 1, Lines 33-49. Column 87, Lines 50-64)**

running the second simulation asynchronously with, and ahead of, the first simulation, the software model of the second simulation being synchronized with the first simulation using a reference clock parameter that limits a maximum number of processor clock periods of the second simulation per period of a reference clock of the hardware environment; **(See section 2.ii above)**

controlling the first simulation of the hardware component from the software debugger through the software model of the second simulation using the inter-process communications protocol; and **(Abstract. Column 1, Lines 33-49. Column 87, Lines 50-64)**

validating the design of the system using the first and second simulations. **(Column 27, Lines 35-40)**

Regarding Claim 16:

Lin discloses A method as claimed in claim 15, further comprising the step of:

connecting the software debugger to inter-process communications protocol connection. **(Abstract. Column 1, Lines 33-49. Column 87, Lines 50-64)**

Regarding Claim 18:

Lin discloses A method as claimed in claim 15, wherein the inter-process communications protocol is TCP/IP and the connection is a TCP/IP socket. **(Abstract. Column 1, Lines 33-49. Column 87, Lines 50-64)**

Regarding Claim 19:

Lin discloses A method as claimed in claim 15, wherein the step of simulating the second hardware component comprises simulating a processor and one or more peripheral devices with which the one or more processors interact directly. **(Figures 1, 2, 3, 5, and 19. Column 27, Lines 45- Column 28, Lines 57)**

Regarding Claim 20:

Lin discloses A method as claimed in claim 15, wherein the first simulation and the second simulation are implemented in separate processing threads. **(Figures 1, 2, 3, 5, and 19. Column 27, Lines 45- Column 28, Lines 57)**

Regarding Claim 21:

Lin discloses A method as claimed in claim 15, wherein the first simulation and the second simulation run asynchronously. **(Figures 1, 2, 3, 5, and 19. Column 27, Lines 45- Column 28, Lines 57)**

Regarding Claim 22:

Lin discloses A method as claimed in claim 15, wherein the first simulation and the second simulation are synchronised with a reference clock. **(Figures 1, 2, 3, 5, and 19)**

Regarding Claim 23:

Lin discloses A method as claimed in claim 15 wherein the first and second simulations are implemented in respective different simulation environments. **(Figures 1, 2, 3, 5, and 19. Column 27, Lines 45- Column 28, Lines 57)**

Regarding Claim 24:

Lin discloses A method as claimed in claim 15, wherein the second hardware component includes embedded processors. **(Column 11, Line 59 – Column 12 Line 2)**

Regarding Claim 25:

Lin discloses A method as claimed in claim 15, wherein the second hardware component includes embedded peripheral devices. **(Column 11, Line 59 – Column 12 Line 2)**

Regarding Claim 26:

Lin discloses A method as claimed in claim 15, wherein the first simulation is implemented using a hardware description language (HDL) simulation environment. **(Figure 26)**

Regarding Claim 28:

Lin discloses A method as claimed in claim 15, wherein the first hardware component is a programmable logic device. **(Column 63, Lines 4-10)**

Regarding Claim 29:

Lin discloses A method for providing an I/O interface for a simulation model to allow the simulation of interactive programs in a hardware environment for use in system validation, the method comprising:

simulating a software element in a first simulation using a software model in a first processing thread in the hardware environment; **(Figures 1, 2, 3, 5, and 19. Column 27, Lines 45- Column 28, Lines 57)**

simulating an embedded input/output device within the simulation model in a second simulation to produce an input/output device model in a second processing thread, the first simulation running ahead of the second simulation, the first and second simulations being synchronized using a reference clock parameter that limits a maximum number of processor clock periods of the first processing thread per period of a reference clock in the hardware environment;; **(See Section 2.ii above)**

connecting the input/output device model to a terminal emulator using an inter-process communications protocol; **(Abstract. Column 1, Lines 33-49. Column 87, Lines 50-64)**

running an interactive program in the terminal emulator to transfer information to the input/output device model, and. **(Abstract. Column 1, Lines 33-49. Column 87, Lines 50-64. Figures 1, 2, 3, 5, and 19)**

polling the input/output device model for the transferred information using the software model. **(Figures 1, 2, 3, 5, and 19. Column 27, Lines 45- Column 28, Lines 57. Column 22, Lines 29-42.)**

validating the design of the system. **(Column 27, Lines 35-40)**

Regarding Claim 30:

Lin discloses A method as claimed in claim 29, the method further comprising: providing separate processing threads for the embedded input/output device to allow concurrent user inputs and outputs. **(Figures 1, 2, 3, 5, and 19. Column 27, Lines 45- Column 28, Lines 57)**

Regarding Claim 31:

Lin discloses A method as claimed in claim 29, wherein the inter-process communications protocol is TCP/IP. **(Abstract. Column 1, Lines 33-49. Column 87, Lines 50-64)**

Regarding Claim 32:

Lin discloses A method as claimed in claim 29, wherein the input/output device is a UART device. **(Figures 1, 2, 3, 5, and 19. Column 27, Lines 45- Column 28, Lines 57)**

Regarding Claim 33:

Lin discloses A method as claimed in claim 29, wherein the input/output device is an Ethernet MAC device. **(Figures 1, 2, 3, 5, and 19. Column 27, Lines 45- Column 28, Lines 57)**

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. **Claim(s) 13 and 27** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Lin in view of Kim et al. "An Integrated Hardware-Software Cosimulation Environment with Automated Interface Generation"**, hereafter referred to as **Kim.**

Regarding Claim 13:

Lin does not explicitly discloses A method as claimed in claim 1, wherein the second simulation is implemented using a C model.

Kim, however, discloses A method as claimed in claim 1, wherein the second simulation is implemented using a C model. **(Introduction, Paragraph 2)**

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize C code for the simulation as discussed in **Kim** for the simulation in **Lin** since C is commonly used higher level programming language as disclosed numerous times in **Kim.**

Regarding Claim 27:

Lin does not explicitly discloses A method as claimed in claim 15, wherein the second simulation is implemented using a C model.

Kim, however, discloses A method as claimed in claim 1, wherein the second simulation is implemented using a C model. **(Introduction, Paragraph 2)**

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize C code for the simulation as discussed in **Kim** for the simulation in **Lin** since C is commonly used higher level programming language as disclosed numerous times in **Kim**.

Conclusion

5. All Claims are rejected.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saif A. Alhija whose telephone number is (571) 272-8635. The examiner can normally be reached on M-F, 11:00-7:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571) 272-22792279. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAA

January 7, 2008

SPE 2128